CLOCK DATA RECOVERY CIRCUITRY WITH DYNAMIC SUPPORT FOR CHANGING DATA RATES AND A DYNAMICALLY ADJUSTABLE PPM DETECTOR

[0059] Clock data recovery (CDR) circuitry can be provided with dynamic support for changing data rates caused by the interfacing of different protocols. The CDR circuitry, which operates in reference clock mode and data mode, can be controlled by two control signals that signal the CDR circuitry to automatically switch between reference clock mode and data mode, to operate only in reference clock mode, or to operate only in data mode. The control signals can be set by a programmable logic device (PLD), by circuitry external to the PLD, or by user input. A dynamically adjustable parts per million (PPM) detector can also be provided in the CDR circuitry to signal when processing of data during the reference clock mode is completed.